

Claims

I claim:

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1. A method of processing packets in a switch comprising:
 - selecting a first queue from at least three queues in a switch based on the cycle number (C) of a cycle;
 - flushing the first queue at the start of the cycle;
 - receiving at least one isochronous packet over a bus during the cycle;
 - placing the packet in a second queue ^{formula} based on the cycle number.

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1 2. The method of claim 1 further comprising:
2 transmitting the packet from the second queue after two cycles.

1 3. The method of claim 1 wherein the first queue is chosen from four queues.

1 4. The method of claim 1 wherein the first queue is associated with a cycle that has a
2 cycle number of C minus 1.

1 5. The method of claim 1 wherein the first queue is the same as the second queue. 112 2nd

1 6. The method of claim 1 wherein the first queue number is equal to the remainder
2 of $(C-1)/n$ wherein n is the number of queues in the switch.

1 7. The method of claim 1 wherein the second queue number is equal to the
2 remainder of $(C+2)/n$ wherein n is the number of queues in the switch.

1 8. The method of claim 1 further comprising:
2 transmitting packets in cycle C from a third queue wherein the queue number of
3 the third queue is equal to the remainder of C/n wherein n is the number of queues in the
4 switch.

1 9. The method of claim 1 further comprising:
2 setting a free pointer in the first queue to 0 at the end of the cycle; and
3 setting a used pointer in the first queue to 0.

1 10. The method of claim 1 further comprising:
2 setting a used pointer in the second queue to 0 at the end of the cycle; and
3 setting a free pointer in the second queue to n.

1 11. A system of processing packets in a bus switch comprising:
2 means for storing data in queues; *Q*
3 means for selecting appropriate queuing means for each set of incoming data; *C*
4 means for directing the set of incoming data to the appropriate queuing means; *B*
5 and
6 means for flushing data from the queuing means. *F*

1 12. The system of claim 11 further comprising means for receiving the incoming data
2 and wherein the incoming data includes isochronous packets.

1 13. A switch in a network comprising:
2 a buffer memory including at least three egress queues; and

3 a processor configured to direct incoming isochronous packets into one of the
4 egress queues based on a cycle number of the switch and configured flush another of the
5 egress queues based on the cycle number.

1 14. The switch of claim 13 wherein the switch is configured to be used with at least
2 one bus.

1 15. The switch of claim 13 wherein the switch is configured to be used with a
2 connection selected from the group: ethernet bus, asynchronous transfer mode bus, and
3 IEEE 1394 standard bus.

1 16. The switch of claim 13 further comprising:
2 at least one ingress port; and
3 at least one egress port
4 wherein each egress port is associated with at least three egress queues.

1 17. The switch of claim 16 wherein the egress queues store data to be transmitted by
2 the processor from each egress port.

1 18. The switch of claim 13 wherein the buffer memory includes four queues.

1 19. The switch of claim 13 wherein the processor is configured to direct the incoming
2 isochronous packets into the egress queue number equal to the remainder of $(C + 2)/n$
3 wherein n is the number of queues in the switch.

1 20. The switch of claim 13 wherein the processor is configured to flush the egress
2 queue number equal to the remainder of $(C - 1)/n$ wherein n is the number of queues in
3 the switch.

1 21. The switch of claim 13 wherein the processor is configured to transmit the
2 isochronous packets from the egress queue number equal to the remainder of C/n wherein
3 n is the number of queues in the switch.